

In the claims:

For the Examiner's convenience, all pending claims are presented below with changes shown.

1 1. (Cancelled)

1 2. (Currently Amended) The CPU of claim 3 + wherein the mapping logic function
2 distributes entries within the TLB throughout the TLB.

1 3. (Currently Amended) A central processing unit (CPU) comprising:
2 a translation lookaside buffering; and
3 a mapping logic function to predict a set index value for the TLB prior to the
4 generation of an effective address, The CPU of claim 1 wherein the mapping logic having
5 comprises a N-bit add modulo 2^N function of base-register bits and offset bits of a virtual
6 address, where N is smaller than the number of bits in a virtual address.

1 4. (Currently Amended) A central processing unit (CPU) comprising:
2 a translation lookaside buffering; and
3 a mapping logic function to predict a set index value for the TLB prior to the
4 generation of an effective address, The CPU of claim 1 wherein the mapping logic having
5 comprises an Exclusive-or of some number of base-register bits and some number of
6 offset bits of a virtual address.

1 5. (Currently Amended) The CPU of claim 4 + further comprising a register
2 interface having one or more registers to control the TLB.

1 6. (Original) The CPU of claim 5 wherein the one or more registers within the
2 register interface chooses an entry within the TLB to be accessed.

1 7. (Currently Amended) A central processing unit (CPU) comprising:
2 a translation lookaside buffering; and
3 a mapping logic function to predict a set index value for the TLB prior to the
4 generation of an effective address. ~~The CPU of claim 1~~ wherein the predicted set index
5 may differ from the effective address without requiring recovery actions if the predicted
6 set index and the effective address differ.

1 8. (Currently Amended) The CPU of claim 7 + wherein mapping logic function
2 includes a first set of bits from instruction and a second set of bits from base and offset
3 addresses.

1 9. (Currently Amended) The CPU of claim 7 + wherein the effective address being
2 mapped is the address of an instruction that is being fetched for execution.

1 10. (Currently Amended) The CPU of claim 7 + wherein the effective address being
2 mapped is the address of data being read or written by the processor.

1 11. (Currently Amended) A central processing unit (CPU) comprising:

2 a translation lookaside buffering; and
3 a mapping logic function to predict a set index value for the TLB prior to the
4 generation of an effective address. ~~The CPU of claim 1 wherein~~ the mapping logic
5 function includes control signals received from the processor and bits received from the
6 generation of the effective address.

1 12. (Original) The CPU of claim 11 wherein the mapping logic combines the
2 signals and the bits using a hash to predict a set to look up the translation for the
3 predicted address.

1 13. (Currently Amended) A method comprising:
2 looking up a register at a register interface; and
3 predicting a set index value for a translation lookaside buffer (TLB) at a mapping
4 logic function having an Exclusive-or of some number of base-register bits and some
5 number of offset bits of a virtual address prior to the generation of an effective address.

1 14. (Original) The method of claim 13 further comprising performing a lookup of
2 the TLB using the predicted set index.

1 15. (Original) The method of claim 13 further comprising calculating an effective
2 address.

1 16. (Original) The method of claim 13 wherein the predicted set index differs
2 from the effective address.

1 17. (Cancelled)

1 18. (Currently Amended) The computer system of claim ~~19~~ 17 wherein the mapping
2 logic function distributes entries within the TLB throughout the TLB.

1 19. (Currently Amended) A computer system comprising central processing unit
2 (CPU) having a mapping logic function to predict a set index value for a translation
3 lookaside buffer (TLB) prior to the generation of an effective address, The computer
4 ~~system of claim 17 wherein~~ the mapping logic function having ~~comprises~~ a N-bit add
5 modulo 2^N function of base-register bits and offset bits of a virtual address, where N is
6 smaller than the number of bits in a virtual address.

1 20. (Currently Amended) The computer system of claim ~~19~~ 17 wherein the mapping
2 logic function comprises an Exclusive-or of some number of base-register bits and some
3 number of offset bits of a virtual address.

1 21. (Currently Amended) The computer system of claim ~~19~~ 17 further comprising a
2 register interface having one or more registers to control the TLB.

1 22. (Original) The computer system of claim 21 wherein the one or more
2 registers within the register interface chooses an entry within the TLB to be accessed.

1 23. (Currently Amended) The computer system of claim 19 ~~17~~ wherein the mapping
2 logic function includes control signals received from the processor and bits received from
3 the generation of the effective address.

1 24. (Original) The computer system of claim 23 wherein the mapping logic
2 combines the signals and the bits using a hash to predict a set to look up the translation
3 for the predicted address.

1 25. (Cancelled)

1 26. (Currently Amended) The computer system of claim 27 ~~25~~ wherein the mapping
2 logic function distributes entries within the TLB throughout the TLB.

1 27. (Currently Amended) A computer system comprising: The computer system of
2 claim 25 wherein
3 central processing unit (CPU) having a mapping logic function to predict a set
4 index value for a translation lookaside buffer (TLB) prior to the generation of an effective
5 address, the mapping logic having comprises a N-bit add modulo 2^N function of base-
6 register bits and offset bits of a virtual address, where N is smaller than the number of
7 bits in a virtual address;
8 a chipset coupled to the CPU and
9 a main memory coupled to the chipset.